

Appln. Serial No. 10/039,045
Amendment Under 37 C.F.R. § 1.312

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

1 1. – 2. (Cancelled)

1 3. (Previously Presented) The method of claim 6, the step of asserting a lock signal further
2 comprising the step of:
3 asserting a split lock signal on the first bus, the split lock signal indicating that the lock
4 request contains two memory address data.

1 4. – 5. (Cancelled)

1 6. (Previously Presented) A method of controlling access to a shared memory of a
2 multiprocessor system, the multiprocessor system comprising a first bus and a second bus
3 coupled to the shared memory, the first bus coupled to a first processor, and the second bus
4 coupled to a second processor, the method comprising the steps of:
5 requesting exclusive access to a first memory location of the shared memory by the first
6 processor;
7 granting exclusive access to the first memory location of the shared memory to the first
8 processor;
9 allowing access to a second memory location of the shared memory to the second
10 processor while the first processor has exclusive access to the first memory location; and
11 storing access request information associated with the exclusive access in a first register
12 in a first memory controller and in a second register in a second memory controller,
13 the step of requesting exclusive access comprising the steps of:
14 asserting a lock signal on the first bus;
15 sending a lock request from the first processor to the first memory controller
16 coupled to the first bus, the second bus, and the shared memory;
17 forwarding the lock request from the first memory controller to a switch; and
18 signaling the first processor to retry the lock request,
19 the step of granting exclusive access comprising the steps of:

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20 signaling the first memory controller by the switch to retry the lock request;
21 assigning exclusive access to the first memory location by the switch;
22 notifying the first memory controller of the exclusive access assigned in the
23 assigning step; and
24 granting exclusive access to the first memory location by the first memory
25 controller responsive to a retry of the lock request by the first processor,
26 the step of assigning exclusive access to the first memory location by the switch
27 comprising the steps of:
28 determining if the first memory location is currently assigned;
29 saving the access request information in a register in the switch if the first
30 memory location is not currently assigned;
31 sending the access request information to the first memory controller; and
32 sending the access request information to the second memory controller.

- 1 7. (Previously Presented) The method of claim 6, the access request information
- 2 comprising:
 - 3 a node ID of the first processor;
 - 4 a cycle ID of the first processor; and
 - 5 memory address data for the first memory location.
- 1 8. (Original) The method of claim 7, the memory address data comprising:
 - 2 a first memory address; and
 - 3 a second memory address,

4 wherein the first memory address can be non-contiguous with the second memory

5 address.
- 1 9. (Previously Presented) The method of claim 6, further comprising the step of:
2 releasing exclusive access to the first memory location.

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1 10. (Previously Presented) A method of controlling access to memory of a multinodal
2 computer system, the multinodal computer system comprising a plurality of multiprocessor
3 nodes, the method comprising the steps of:

4 requesting exclusive access to a first memory location of a shared memory in a first
5 multiprocessor node of the plurality of multiprocessor nodes by a first processor of the first
6 multiprocessor node;

7 granting exclusive access to the first memory location of the shared memory to the first
8 processor;

9 allowing access to a second memory location of the shared memory to a second processor
10 of a second multiprocessor node of the plurality of multiprocessor nodes while the first processor
11 has exclusive access to the first memory location;

12 communicating between the multiprocessor nodes through a switch; and

13 sending, by the switch, access request information associated with the exclusive access of
14 the shared memory of the first multiprocessor node to the second multiprocessor node.

1 11. (Previously Presented) The method of claim 10, the requesting step comprising:
2 asserting a lock signal on a first bus, the first bus coupling the first processor and a first
3 memory controller of the first multiprocessor node; and

4 sending a lock request to the first memory controller;

5 forwarding the lock request from the first memory controller to the switch, the switch

6 coupled to each of the plurality of multiprocessor nodes.

1 12. (Previously Presented) The method of claim 11, the shared memory comprising:
2 a first memory coupled to the first memory controller; and
3 a second memory coupled to a second memory controller in the second multiprocessor
4 node of the plurality of multiprocessor nodes.

1 13. (Original) The method of claim 12, the step of asserting a lock signal comprising the step
2 of:

3 asserting a split lock signal on the first bus, the split lock signal indicating that the lock
4 request contains a first memory address data and a second memory address data.

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1 14. (Original) The method of claim 13, the first memory address data referencing the first
2 memory and the second memory address data referencing the second memory.

1 15. (Original) The method of claim 13, the first memory address data referencing the second
2 memory and the second memory address data referencing the first memory.

1 16. (Previously Presented) The method of claim 11, the step of requesting exclusive access
2 further comprising:
3 signaling the first processor to retry the lock request.

1 17. (Previously Presented) The method of claim 11, the step of granting exclusive access
2 comprising the steps of:
3 signaling the first memory controller to retry the lock request;
4 assigning exclusive access to the first memory location by the switch;
5 notifying the first memory controller of the exclusive access assigned in the assigning
6 step; and
7 assigning exclusive access to the first memory location by the first memory controller
8 responsive to a retry of the lock request by the first processor.

1 18. (Previously Presented) The method of claim 17, the step of assigning exclusive access to
2 the first memory location by the switch comprising the steps of:
3 determining if the first memory location is currently assigned;
4 saving the access request information associated with the exclusive access if the first
5 memory location is not current assigned; and
6 broadcasting the access request information to each memory controller of each of the
7 plurality of multiprocessor nodes.

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1 19. (Previously Presented) The method of claim 18, the access request information
2 comprising:

3 a node ID of the first multiprocessor node;
4 a cycle ID of the first processor; and
5 a memory address data for the first memory location.

1 20. (Original) The method of claim 10, further comprising the step of:
2 releasing exclusive access to the first memory location.

1 21. (Cancelled)

1 22. (Previously Presented) A computer system for utilizing a shared memory, the computer
2 system comprising:

3 a first multiprocessor node, comprising:
4 a first processor bus;
5 a first processor, coupled to the first processor bus, the first processor comprising:
6 circuitry to generate an exclusive access request for a first memory

7 location,
8 a second processor bus;
9 a second processor, coupled to the second processor bus, the second processor
10 adapted to:

11 request access to a second memory location;
12 a first memory;
13 a first memory controller, coupled to the first processor bus, the second processor
14 bus, and the first memory, the first memory controller adapted to:
15 allow exclusive access to the first memory location by the first processor;

16 and
17 allow access to the second memory location by the second processor while
18 the first processor has exclusive access to the first memory location;

19 a second multiprocessor node, comprising:
20 a third processor bus;

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21 a third processor, coupled to the third processor bus, the third processor adapted
22 to:
23 request access to a third memory location;
24 a second memory;
25 a second memory controller, coupled to the third processor bus, and the first
26 memory, the second memory controller adapted to:
27 allow exclusive access to the first memory location by the first processor;
28 allow access to the second memory location by the second processor while
29 the first processor has exclusive access to the first memory location; and
30 allow access to the third memory location by the third processor while the
31 first processor has exclusive access to the first memory location; and
32 a switch, coupled to the first memory controller and the second memory
33 controller, for switching transactions between the first multiprocessor node and the second
34 multiprocessor node.

- 1 23. (Original) The computer system of claim 22, the first memory location comprising:
2 a first portion in the first memory; and
3 a second portion in the second memory.
- 1 24. (Original) The computer system of claim 22,
2 wherein the first memory location is in the first memory, and
3 wherein the second memory location is in the first memory.
- 1 25. (Original) The computer system of claim 22,
2 wherein the first memory location is in the first memory, and
3 wherein the third memory location is in the first memory.
- 1 26. (Original) The computer system of claim 22,
2 wherein the first memory location is in the second memory, and
3 wherein the third memory location is in the second memory.

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- 1 27. (Original) The computer system of claim 22,
2 wherein the first memory location is in the second memory, and
3 wherein the third memory location is in the first memory.
- 1 28. (Original) The computer system of claim 22, the switch comprising:
2 a lock register for storing a lock control information.
- 1 29. (Original) The computer system of claim 28, the lock control information comprising:
2 a node ID corresponding to the first processor;
3 a cycle ID corresponding to the first processor; and
4 a first memory address corresponding to the first memory location.
- 1 30. (Original) The computer system of claim 29, the lock control information further
2 comprising:
3 a second memory address corresponding to the first memory location.
- 1 31. (Previously Presented) The computer system of claim 29, the switch comprising:
2 circuitry to signal the first memory controller to retry allowing exclusive access to the
3 first memory location by the first processor;
4 circuitry to arbitrate among requests for exclusive access to the first memory location;
5 circuitry to broadcast the lock control information to the first memory controller and the
6 second memory controller.
- 1 32. (Original) The computer system of claim 31, the first memory controller further
2 comprising:
3 circuitry to signal the first processor to retry the exclusive access request;
4 circuitry to shadow the lock control information broadcast by the switch; and
5 the second memory controller further comprising:
6 circuitry to shadow the lock control information broadcast by the switch.

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1 33. (Original) The computer system of claim 30, wherein the first memory address can be in
2 either the first memory or the second memory, and
3 wherein the second memory address can be in either the first memory or the second
4 memory.

1 34. (Previously Presented) A method of controlling access to a shared memory of a
2 multiprocessor system, the multiprocessor system comprising a first bus and a second bus
3 coupled to the shared memory, the first bus coupled to a first processor, and the second bus
4 coupled to a second processor, the method comprising the steps of:

5 requesting exclusive access to a first memory location of the shared memory by the first
6 processor;

7 granting exclusive access to the first memory location of the shared memory to the first
8 processor;

9 allowing access to a second memory location of the shared memory to the second
10 processor while the first processor has exclusive access to the first memory location;

11 wherein requesting exclusive access comprises:

12 sending a lock request from the first processor to a first memory controller coupled to the
13 shared memory;

14 forwarding the lock request from the memory controller to a switch; and

15 the switch broadcasting lock request information to the first memory controller and at
16 least another memory controller.

1 35. (Previously Presented) The method of claim 34, further comprising:
2 each of the first memory controller and at least another memory controller storing the
3 lock request information.

1 36. (Previously Presented) The method of claim 35, further comprising the switch storing the
2 lock request information in a register in the switch,
3 wherein the memory controllers also store the lock request information in respective
4 registers in the memory controllers.

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1 37. (Previously Presented) The method of claim 6, wherein the access request information in
2 the second register in the second memory controller is a shadow copy of the access request
3 information in the first register in the first memory controller.

1 38. (Previously Presented) The method of claim 10, further comprising:
2 the switch forwarding the access request information to a second memory controller in
3 the second multiprocessor node; and
4 the second memory controller storing the access request information in the second
5 memory controller.

1 39. (Previously Presented) The method of claim 10, further comprising:
2 storing the access request information in a first register of a first memory controller in the
3 first multiprocessor node and in a second register in a second memory controller in the second
4 multiprocessor node.

1 40. (Previously Presented) The method of claim 39, further comprising storing the access
2 request information in a register in the switch,
3 wherein the access information in the first register of the first memory controller and in
4 the second register of the second memory controller are shadow copies of the access request
5 information in the register of the switch.

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- 1 41. (Previously Presented) A multiprocessor system comprising:
 - 2 a plurality of multiprocessor nodes, each of the multiprocessor nodes comprising:
 - 3 a shared memory;
 - 4 a processor to request exclusive access of a memory location in the shared
 - 5 memory;
 - 6 a memory controller to forward access request information associated with the
 - 7 exclusive access from the multiprocessor node for storage of the access request information in
 - 8 another multiprocessor node, the memory controller including a register; and
 - 9 a switch coupled to the multiprocessor nodes, the switch to receive the access request
 - 10 information and to send the access request information to the multiprocessor nodes for storage of
 - 11 the access request information in the respective registers of the memory controllers.
- 1 42. (Currently Amended) The multiprocessor system of claim [[42]] 41, wherein the switch
2 includes a register to store the access request information,
3 wherein the access request information in the registers of the respective memory
4 controllers are shadow copies of the access request information in the register of the switch.